APPLICATION

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TITLE: DYNAMIC MULTIPHASE OPERATION

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DYNAMIC MULTIPHASE OPERATION

TECHNICAL FIELD

[0001] This invention relates to output regulators.

BACKGROUND

[0002] Output regulators are employed in numerous machines and devices including virtually every electronic device. An output regulator typically converts unregulated input power to one or more regulated outputs for supplying power to circuits within the machine or device. The regulated outputs are most commonly regulated voltage, but regulated current and regulated power may also be generated. The output regulator may be integrated into the machine or device, or the output regulator may be a separate assembly that is assembled to machine or device. Several characteristics of output regulators may be used to judge the quality of a particular design including operating characteristics such as power density, efficiency, output regulation, and transient response. Improvements in the operating characteristics of output regulators are desirable so that machines and devices that use output regulators may be improved such as by being made smaller, requiring less power, having improved accuracy and reliability, or having improved operation during transient conditions.

SUMMARY

[0003] In one aspect, a control system for controlling a multiphase output regulator having a regulated DC output and operating at a switching frequency. The multiphase output regulator including at least two switch arrays to generate individually controllable output phases that combine to form the regulated DC output. The control system comprising a digital controller operable at a sampling frequency greater than the switching frequency. The digital controller responsive to a sense signal corresponding to the regulated output, to generate array duty cycle signals to control each of the switch arrays. The digital controller to control the array duty cycle signals at the sampling frequency and to dynamically set a phase interval between each of the output phases.

[0004] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0005] FIG. 1 is a block diagram of an aspect of a multiphase output regulator.

[0006] FIG. 2 is a block diagram of an aspect of a multiphase output regulator.

[0007] FIG. 3 is a block diagram of an aspect of a switch assembly.

[0008] FIG. 4A is a graph of phase waveforms corresponding to aspect of a multiphase output regulator.

[0009] FIG. 4B is a graph of phase waveforms corresponding to aspect of a multiphase output regulator.

[0010] FIG. 4C is a graph of phase waveforms for a conventional multiphase output regulator.

[0011] FIG. 4D is a graph of phase waveforms corresponding to aspect of a multiphase output regulator.

[0012] FIG. 5 is a flow diagram of an operation for controlling a multiphase output regulator.

[0013] FIG. 6 is a block diagram of a digital controller for generating a duty cycle signal.

[0014] FIG. 7 is a graphical representation of voltage ranges spaced about a nominal output voltage, Vout.

[0015] FIG. 8 is a timing diagram of waveforms showing quantization error associated with an aspect of a digital controller.

[0016] Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0017] Figure 1 shows a multiphase output regulator 10 for supplying regulated power to a load 12. Although, the multiphase output regulator 10 is described as having a buck topology, any type of topology may be used such as boost, flyback (buck-boost), Cuk, Sepic, and Zeta. The multiphase output regulator 10 may include a power array 20 to convert an unregulated DC voltage, such as Vin, to multiple output phases 18 that have a dynamically controlled phase relationship. Each of the output phases 18 may include a variable pulse width power signal that may be skewed in time, relative to the other output phases by a phase interval. In addition, the quantity of active output phases may be dynamically controlled. For example, the power array 20 may generate up to "N" different output phases such as 8 output phases 18. During one operating condition, 4 output phases may be active and spaced at 90 degree time intervals. Then, while the multiphase output regulator 10 operates, another of the output phases 18 may be activated and the 5 active output phases be dynamically controlled to be spaced at 72 degree time intervals.

[0018] The power array 20 may generate current sense signals, Is, corresponding to each of the output phases 18. Multiple output filters 24 corresponding to the output phases 18 may filter the output phases 18 to generate filtered outputs 25 that may be combined to form a regulated output 26. Each of the output filters 24 may include an output inductor and an output capacitor. By skewing two or more of the output phases 18, the ripple voltage of the regulated output may be reduced, and the ripple frequency may be increased leading to a reduction in the size of the output filters. The regulated output 26 is preferably a DC voltage output and may be any output characteristic including voltage, current, and power. The unregulated voltage, Vin, may be any form of input power such as alternating current (AC) voltage and DC voltage. For an AC input voltage a rectification stage (not shown) may be included to convert the AC voltage to the DC input voltage, Vin. An output sensor 28 may sense the regulated output 26 and send a feedback signal 16 to a digital controller 14. Any type of output sensor 28 may be employed to sense the output. The digital controller 14 may, in response to receiving input signals such as the feedback signal 16, generate one or more control signals to drive the power array 20. Other input signals may include the current sense signals Is from the power array 20. The control signals in the digital controller

14 may include a duty cycle signal, a phase interval signal, and an inertializer signal. The duty cycle signal may control the operating frequency, variable frequency versus fixed frequency operation, the number of output phases generated and the duty cycle generated by the active output phases 18. The phase interval signal may control the phase angle of each of the output phases 18. The inertializer signal may control turn-on of the power array 80 to increase the current flowing through the output inductor to the steady-state level to reduce transients in the regulated output during turn-on. The digital controller 14 may generate drive signals based on the control signals to drive the power array 20. The digital controller 14 may operate at a sampling frequency greater than the switching frequency of the multiphase output regulator. The digital controller 14 may operate at a sampling frequency that is greater than the switching frequency such as a factor of 32, although the frequency of the sampling frequency is non-limiting. The digital controller 14 may be implemented in any programmable digital device such as a real time digital signal processor.

[0019] Figure 2 shows an aspect of a multiphase output regulator 50 for supplying power to a load 62. The multiphase output regulator 50 may include a power array 52 having from two to "N" switch arrays 54 for generating phased outputs from

a DC input voltage. Each of the switch arrays 54 may receive one or more control signals to control the operating characteristics of the switch arrays 54 such as duty cycle, operating frequency, enable/disable, and start-up operation.

[0020] Figure 3 shows an aspect of a switch array 80. The switch array 80 may generate a pulse width modulated output in response to one or more drive signals. A pair of power switches 82 and 84 may be connected in a half-bridge configuration between two voltage sources. The power switches 82 and 84 may be driven by the drive signals to operate in a switching mode to generate the pulse width modulated output. Any type of power switch may be used such as MOSFETs, BJTs, MCTs, IGBTs, and RF FETs. Each of the power switches 82 and 84 may comprise one or more parallel power switches.

[0021] Drivers 88 and 89 may buffer the drive signals from the digital controller 14 to the power switches 82 and 84. Any type of driver may be used.

[0022] A current sense circuit 85 may sense current flowing to the output or through the power switches 82 and 84. Any type of current sense circuit 85 may be used such as resistive, transformer-resistor, Hall effect, and sensing voltage across the channel of a FET device.

[0023] The power array 52 may include output filters 56 corresponding to each of the switch arrays 54. The output

filters 56 filter the phase outputs of the switch arrays to generate the regulated output. Each output filter 56 may include an output inductor 58. A single output capacitor 60 is preferably connected to the combined output of the output filters 56. However, the output capacitors 60 may be distributed so that each output filter 56 includes an output capacitor 60.

[0024] A digital controller 64 may generate the control signals to control the flow of power through the power array 52 to the load 62. The digital controller 64 may include a duty cycle controller 66 to determine, as a function of a feedback signal from the load 62, a regulator duty cycle to maintain the regulated output in regulation. The feedback signal may sample any output characteristic such as voltage, current, and power. The duty cycle controller 66 may also control the duty cycle as a function of the current, Is, flowing through the output inductor 58 or the power switches 82 and 84. The duty cycle controller 66 may implement either voltage mode control or current mode control. Also, the duty cycle controller 66 may implement fixed frequency or variable frequency operation. The duty cycle controller 66 may sample the feedback signal and Is at a sampling frequency greater than the switching frequency of the multiphase output regulator 50.

[0025] Switch controllers 68 may determine and control the power array operating characteristics such as the quantity of phases to generate the duty cycle for each of the activated switch arrays 54, and a phase interval between each of the activated output phases 54, where the phase interval is the time offset between the leading edges or the trailing edges of the pulses for each of the output phases 54 that are active. Under steady-state operating conditions the phase interval as measured between the leading edges of the pulses or measured between the trailing edges of the pulses is approximately equal. There may be a one to one correspondence between the switch controllers 68 and the switch arrays 54. However, the scope of the invention includes controlling either all or a subset of the switch arrays 54 with a single switch controller 68. The drive signals for each of the switch arrays 54 may be set as a function of the duty cycle signal from the duty cycle controller 66. Some of the other power array operating characteristics that the switch controllers 68 may determine and control include the quantity of switch arrays 54 to enable, and the switching frequency of the multiphase output regulator 50, where the switching frequency is the frequency of the individual output phases 54. The switch controllers 68 may determine the power array operating characteristics based on any regulator criteria such as output current, power switch

current for any of the switch arrays, output inductor current, output voltage, output ripple voltage, input voltage, noise generation, and power consumption in discrete components, circuits, or the entire output regulator.

[0026] Figure 4A shows waveforms of three of the N output phases 54 for an aspect of changing from 2 phase operation to 3 phase operation. The remaining output phases, φ4 to φN remain inactive. The array controller 68 may enable phases φ1 and φ2 of the output phases 54 to each operate at a duty cycle of 33.3% with a phase interval of t1. The multiphase output regulator 50 may operate with only phases φ1 and φ2 active for any period of time. Then, the array controller 68 may enable phase φ3 of the output phases 54 and set each of the output phases, φ1, φ2, and φ3 to a duty cycle of 33.3% with a phase interval of t2. The array controller 68 dynamically changes the phase interval of the output phases 54 to adjust for increasing the number of active output phases 54 from 2 to 3.

[0027] The array controller 68 may also control the current flowing through individual ones of the output inductors 58. In one aspect, when enabling one or more additional phase outputs, the array controller 68 may control the corresponding switch array 54 to ramp up the current flowing through the corresponding output inductor 58 to minimize the transient response time as the currents flowing through the output

inductors 58 of the active output filters 56 settle out to steady-state levels.

[0028] Figure 4B shows waveforms of the operation of an aspect of the multiphase output regulator 50 during an output load change. At time ta the output load, I_{load}, increases, and the array controller 68 may set all or a subset of the output phases to 100% duty cycle to cause the output current to quickly increase, reducing transient changes in the output voltage. After a period of time, the array controller 68 may dynamically reintroduce the phase relationships between each of the output phases. For example, the array controller may control the leading edges of the drive signals to dynamically set the phase interval between each of the output phases. The trailing edges of the drive signals are then controlled to maintain the regulated output within the regulation limits. In another exemplary system, the array controller 68 may control the trailing to set the phase interval, and control the leading edges to maintain the regulated output in regulation. The array controller 68 may operate similarly when the output load, I_{load}, decreases (not shown). Here, the array controller may set all or a subset of the output phases to 0% duty cycle to cause the output current to quickly decrease, reducing transient changes in the output voltage.

[0029] Figure 4C shows waveforms of the operation of a conventional multiphase output regulator having four output phases. Conventional multiphase output regulators generally control only the trailing edge of the drive signals. The trailing edge is controlled to maintain the regulated output in regulation. The leading edges of the drive signals for each of the output phases are generally fixed in relation to each other. As the total quantity of output phases is changed, the phase relationship between the phases remains static. For example, in a conventional multiphase output regulator having four output phases, the output phases may be spaced apart by 90 degrees so that the leading edges occur at 0 degrees, 90 degrees, 180 degrees, and 270 degrees. When one of the output phases is disabled, the remaining output phases do not shift relative to each other so that the leading edges may occur at 0 degrees, 90 degrees, and 180 degrees. In addition, during a load change, the length of the conduction time for each of the pulses may be lengthened, but the time relationship between the leading edges is typically maintained static and the time relationship between the trailing edges is also typically maintained static.

[0030] In contradistinction, the phase interval of the multiphase output regulator 50 may be adjusted dynamically by controlling the leading or trailing edges of the drive

signals. For example, when the quantity of output phases is changed, the phase interval between each of the output phases may be dynamically changed such as shifting the leading edges from 0 degrees, 90 degrees, 180 degrees, and 270 degrees, to 0 degrees, 120 degrees, and 240 degrees when one of four output phases is disabled.

[0031] Figure 4D shows another aspect of the multiphase output regulator 50. The array controller 68 may set multiple switch arrays to the same phase such as setting the output phase pairs φ1-φ4, φ2-φ5, and φ3-φ6 to approximately the same duty cycle. The array controller 68 may also apply dithering to the active output phases. The array controller 68 may generate a minimum increment resolution of the duty cycle that is equal to "x1", and by applying dithering to an output phase or a complementary output phase, the average of the generated pulse may be stretched by any fractional portion of "x1". In one dithering method, a selected number of pulses within an output phase may be stretched by an integer "N" number of increments, and the remaining pulses within the output phase may be stretched by an integer "N-1" or "N+1" number of increments to generate a pulse that is fractionally stretched.

[0032] Figure 5 shows an aspect of the operation of a multiphase output regulator. At step 100, sense a regulated output of the multiphase output regulator. At step 102,

generate a digital feedback signal as a function of the regulated output. At step 104, determine a duty cycle at which to convert power from an input source to the regulated output. Continuing to step 106, determine a quantity of output phases to generate. At step 108, determine a quantity of switch arrays to enable. One or more switch arrays may be used to generate each of the output phases. For example, two switch arrays may be used for each of four output phases leading to a total of eight switch arrays. Continuing to step 110, determine an array duty cycle for each of the switch arrays based on the regulator duty cycle. At step 112, determine a phase interval to separate the pulses of each of the output phases. The phase interval may be referenced to any portion of the output phase waveform such as the leading and trailing edges of the pulse. At step 114, precondition the output inductor currents that correspond to the switch arrays that change operating state from either active to inactive, or from inactive to active. At step 118, apply dithering to the active output phases.

[0033] Figure 6 shows an aspect of a digital controller 200. The digital controller 200 may include a duty cycle controller 202 to determine a duty cycle for operating the switch arrays 54. The duty cycle controller 202 may include a duty cycle estimator 952 to generate nominal duty cycle signals and an

adjust determiner 954 to determine an adjustment value, ADJ, to combine with the nominal duty cycle signals.

[0034] The duty cycle estimator 952 may generate nominal duty cycle signals, Up* and Down*, that correspond to nominal steady-state values from which to generate a current duty cycle for the switching regulator. The duty cycle estimator 952 may be used for generating nominal duty signals in operating states such as PWM, variable frequency, quasi-resonant mode, and energy saving discontinuous mode. However during a hysteretic control operating state, the duty cycle estimator 952 is preferably not used for computing the nominal duty cycle. Instead during hysteretic control, the duty cycle may be directly related to the error signal so that when the error signal is in one state the duty cycle is set to the ON state (up), and when the error signal is in the other state the duty cycle is set to the OFF state (down). The duty cycle estimator 952 may generate the nominal duty cycle signals as a function of input signals such as an error signal, a UD pulse, and a delay control. The error signal may represent the error between the regulated output and a reference. Power switches in the switching regulator may be operated at the current duty cycle to control the conversion of energy from an input source, Vin, to the load 212. For example, in a switching regulator having a buck topology and fixed frequency

operation, the nominal duty cycle signal Up* may be approximately equal to a value that corresponds to the ratio of the output voltage to the input voltage. In another aspect, the nominal duty cycle may be determined by computing a running average of the duty cycle over a predetermined quantity of switching cycles. In another aspect, the nominal duty cycle may be determined by incrementing or decrementing the prior nominal duty cycle based on the amplitude of the error signal. During fixed frequency operation, the combination of the nominal steady-state values may correspond to the total switching period of the switching regulator such as 1 usec for a 1 MHz switching frequency.

[0035] The adjust determiner 954 may determine an adjustment value, ADJ, to combine with the nominal duty cycle signals to generate adjusted duty cycle signals, Up and Down. The adjust determiner 954 may generate the adjustment value as a function of the error signal as well as other signals from the switching regulator. The adjust determiner 954 may generally be used for any operating state except hysteretic control. Since in the hysteretic control operating state, the duty cycle is either 100% ON or 100% OFF, no adjustment value is required. In one aspect, the adjustment value for the PWM state and the energy saving discontinuous mode may be computed as follows:

$$ADJ_k = g(e_k) + h(trend_k)$$
$$Up_k = Up^* - ADJ_k * FAC^{on}$$
$$Down_k = Down^* + ADJ_k * FAC^{off}$$

where FAC may be determined based on the nominal duty cycle,

$$g(e_k) = \begin{cases} 0 & if \quad |e_k| < A1 \\ sign(e_k) * \Delta_1 & if \quad A1 \le |e_k| < A2 \\ sign(e_k) * \Delta_2 & if \quad A2 \le |e_k| < A3 \end{cases}$$

$$h(trend_k) = \begin{cases} 0 & if \quad |trend_k| < 1 \\ trend_k & if \quad |trend_k| \ge 1 \end{cases}$$

$$trend_k = F_{slope} * \overline{e_k - e_{k-n}}$$

where F_{slope} is a constant, $\overline{e_k - e_{k-n}}$ is an average of the slope of the waveform where the slope is the error difference from the "n" prior cycles, where "n" is the number of samples in a switching period, and

A1, A2, and A3 are defined in Figure 7 which shows voltage levels of a voltage slicer for generating the error signal. The voltage levels may be selected to define voltage ranges that are approximately centered around a nominal voltage level for the output voltage, Vout.

[0036] Δ_1 and Δ_2 are loop gains which may be selected at the sampling rate and may have values based on the amplitude of the error signal. The values of the loop gains, Δ_1 and Δ_2, may be selected to be related such as Δ_2 being approximately equal

to two times Δ_1. The loop gain of the digital controller may be changed adaptively at any rate up to and including the sampling rate. Each of the loop gains may be dynamically changed as a function of any parameter of the output regulator such as the voltage range of the error signal, the voltage range of the regulated output, and the duty cycle.

[0037] The loop compensation of the digital controller may be described by the ratio of $g(e_k)$ to $h(trend_k)$, which may be expressed generally as (A*e(k)/B*e'(k)). The loop compensation may be controlled at any rate up to and including the sampling frequency. In one aspect, the constant F_{slope} may be adaptively changed to change the loop compensation. The loop compensation may be dynamically changed as a function of any parameter of the output regulator such as the voltage range of the error signal, the voltage range of the regulated output, and the duty cycle.

[0038] A combiner 956 may combine the nominal duty cycle signals with the adjustment value to generate the adjusted duty cycle signals. In one aspect, the adjusted duty cycle signals may be used as counter limits for generating a UD pulse.

[0039] One or more switch controllers 204 may receive the adjusted duty cycle signal and generate drive signals for controlling each of the switch arrays 54 of the power array

52. Each of the switch controllers 204 may control the power array operating characteristics such as the quantity of output phases to generate, the quantity of switch arrays 54 to generate each output phase, and a phase interval between each of the activated output phases 54, where the phase interval is the time offset between the leading edges of the pulses for each of the output phases 54 that are active. Each switch controller 204 may receive a current sense signal, CL_N, from a corresponding switch array 54, and control the drive signals as a function of the current sense signal.

[0040] A counter 958 may generate the UD_D pulse as a function of a clock signal, CLOCK, and the adjusted duty cycle signals. The UD_D pulse preferably is a binary signal representing a varying on-time for driving the power switches of the switching regulator. The counter 958 may count a quantity of clock cycles set by the counter limits to generate the "on-time" and "off-time" of the UD_D signal. For example, the Up portion of the adjusted duty cycle signal may set the counter limit for the on-time and the Down portion of the adjusted duty cycle signal may set the counter limit for the off-time. Preferably, a single counter generates the UD_D signal in response to a single counter limit signal including both the Up and Down information. The UD_D pulse may include a quantization error related to the pulse resolution being

limited by the frequency of the clock signal. Figure 8 shows an example of quantization error in which a UD_D pulse 970 that is generated from a clock signal 972 and an adjusted duty cycle signal 974 may have a quantization error 976 related to the frequency of the clock signal.

[0041] A delay line 960 may generate drive signals, UD_A pulse, that finetune the pulse width of the UD_D pulse generated by the counter 958 to reduce the quantization error. The UD_A pulse preferably has an "on" level and an "off" level and may have a varying pulse width to represent an on-time for driving the power switches of the switch array 54. The delay line 960 may, in response to receiving the UD_D pulse and a delay control signal, generate the UD_A pulse having a duty cycle that approximates the pulse width corresponding to the adjusted duty cycle signals. The delay line 960 may delay either edge of the UD_D pulse to generate the UD_A pulse. For example, in one aspect the UD_D pulse may be generated having a pulse width shorter than the corresponding adjusted duty cycle, and then the delay line 960 may delay the trailing edge to generate the UD_A pulse. In another aspect, the UD_D pulse may be generated having a pulse width longer than the corresponding adjusted duty cycle, and then the delay line 960 may delay the leading edge to generate the UD_A pulse.

[0042] A delay control 962 may generate the delay control signal as a function of the UD_D pulse and the adjusted duty cycle signals. The delay control signal may preferably be a multi-bit signal.

[0043] A phase controller 964 may monitor the UD_A pulse and in response control the counter 958 and the delay control 962 to set the phase characteristics of the power array 52. The phase characteristics may include the quantity of output phases, the quantity of active switch arrays 54 per output phase, and the phase interval between output phases.

[0044] A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.